Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-19 (Canceled)

Claim 20 (New): A drive circuit comprising:

an input node for receiving data;

an output node;

a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the input node;

a second MOS transistor of the first conductivity type, the second MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential level; and

a resistor which comprises a third MOS transistor of the first conductivity type, the third MOS transistor having a source connected to a source node supplied with a source potential level, a drain connected to the source of the second MOS transistor and a gate connected to a ground node supplied with a ground potential level.

Claim 21 (New): The drive circuit according to claim 20, further including a fourth MOS transistor of a second conductivity type, the fourth MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the input node.

Claim 22 (New): The drive circuit according to claim 20, wherein the second MOS transistor supplies a constant current to the output node.

Claim 23 (New): A drive circuit comprising:

an input node for receiving data;

an output node;

a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the input node;

a second MOS transistor of the first conductivity type, the second MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential level; and

a resistor which comprises a third MOS transistor of the first conductivity type, the third MOS transistor having a source connected to a ground node supplied with a ground potential level, a drain connected to the source of the second MOS transistor and a gate connected to a source node supplied with a source potential level.

Claim 24 (New): The drive circuit according to claim 23, further including a fourth MOS transistor of a second conductivity type, the fourth MOS transistor having a source connected to a source node supplied with a source potential, a drain connected to the output node, and a gate connected to the input node.

Claim 25 (New): The drive circuit according to claim 23, wherein the second MOS transistor supplies a constant current to the output node.

Claim 26 (New): A drive circuit comprising:

a source node supplied with a source potential level;

a ground node supplied with a ground potential level;

a data input node for receiving data;

an output node to which a light-emitting device is connected;

a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the data input node;

a second MOS transistor of a second conductivity type, the second MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the data input node;

a third MOS transistor of the first conductivity type, the third MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate

supplied with a predetermined potential level between the source potential level and the ground potential level; and

a resistor which comprises a fourth MOS transistor of the first conductivity type, the fourth MOS transistor having a source connected to the source node, a drain connected to the source of the third MOS transistor and a gate connected to the ground node.

Claim 27 (New): The drive circuit according to claim 26, wherein the third MOS transistor supplies a constant current to the output node.

Claim 28 (New): A drive circuit comprising:

a source node supplied with a source potential level;

a ground node supplied with a ground potential level;

a data input node for receiving data;

an output node to which a light-emitting device is connected;

a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the data input node;

a second MOS transistor of a second conductivity type, the second MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the data input node;

a third MOS transistor of the first conductivity type, the third MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential which is less than the source potential level and more than the ground potential level; and

a resistor connected between the source node and the source of the third MOS transistor.

Claim 29 (New): A drive circuit comprising:

a source node supplied with a source potential level;

a ground node supplied with a ground potential level;

a data input node for receiving date;

an output node to which a light-emitting device is connected;

a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate supplied with a predetermined potential level which is less than the source potential level and more than the ground potential level;

a second MOS transistor of the first conductive type, the second MOS transistor having a source connected to the source node, a drain connected to the source of the first MOS transistor, and a gate connected to the data input node; and

a third MOS transistor of a second conductive type, the third MOS transistor having a source connected to the ground node, a drain connected to the output node,

and a gate connected to the data input node.

Claim 30 (New): The drive circuit according to claim 29, wherein the first MOS transistor supplies a constant current to the output node.

Claim 31 (New): A drive circuit comprising:

a constant current generator comprising

an operational amplifier having an inversion terminal to which a reference voltage is applied, a non-inversion terminal and an output terminal,

a first MOS transistor of a first conductivity type, wherein the first MOS transistor has a source, a drain connected to the non-inversion terminal of the operational amplifier and a gate connected to the output terminal of the operational amplifier, and

a second MOS transistor of the first conductivity type, wherein the second MOS transistor has a source connected to a source node supplied with a source potential, a drain connected to the source of the first MOS transistor and a gate connected to a gate node supplied with a gate potential level; and

a data line driver comprising

an input node for receiving data,

an output node,

a third MOS transistor of the first conductivity type, wherein the third MOS

transistor has a source, a drain connected to the output node, and a gate connected to the input node,

a fourth MOS transistor of the first conductivity type, wherein the fourth MOS transistor has a source, a drain connected to the source of the third MOS transistor, and a gate connected to the gate of the first MOS transistor, and

a resistor connected between the source of the fourth MOS transistor and the source node.

Claim 32 (New): The drive circuit according to claim 31, wherein the resistor comprises a MOS transistor.

Claim 33 (New): The drive circuit according to claim 31, wherein the fourth MOS transistor supplies a constant current to the output node.

Claim 34 (New): The drive circuit according to claim 31, wherein the data line driver further comprises a fifth MOS transistor of a second conductivity type, the fifth MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the input node.

Claim 35 (New): A drive circuit comprising:

a constant current generator comprising

an operational amplifier having a non-inversion terminal to which a reference voltage is applied, an inversion terminal and an output terminal,

a first MOS transistor of a first conductivity type, wherein the first MOS transistor has a source, a drain connected to the inversion terminal of the operational amplifier and a gate connected to the output terminal of the operational amplifier, and

a second MOS transistor of the first conductivity type, wherein the second MOS transistor has a source connected to a ground node supplied with a ground potential level, a drain connected to the source of the first MOS transistor and a gate connected to a source node supplied with a source potential level; and

a data line driver comprising

an input node for receiving data,

an output node,

a third MOS transistor of the first conductivity type, wherein the third MOS transistor has a source, a drain connected to the output node, and a gate connected to the input node,

a fourth MOS transistor of the first conductivity type, wherein the fourth MOS transistor having a source, a drain connected to the source of the third MOS transistor, and a gate connected to the gate of the first MOS transistor, and

a resistor connected between the source of the fourth MOS transistor and the ground node.

Claim 36 (New): The drive circuit according to claim 35, wherein the resistor comprises a MOS transistor.

Claim 37 (New): The drive circuit according to claim 35, wherein the fourth MOS transistor supplies a constant current to the output node.

Claim 38 (New): The drive circuit according to claim 35, further including a fifth MOS transistor of a second conductivity type, the fifth MOS transistor having a source connected to the source node, a drain connected to the output node, and a gate connected to the input node.